Exploration of SSL Architecture in Designing Future Communication Systems

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Abstract— Parity bit generators are indispensable in modern communication system. From the very beginning different types of parity generators are being fabricated using conventional CMOS technology. Hamming code is one such excellent example of modern parity bit generators. But the fact is that CMOS technology is facing tremendous physical challenges from the scaling point of view. In order to compensate this short comings of CMOS several new technologies has evolved. One such technology is Spintronics technology. The Spintronics technology is now used to model Boolean logics, thereby the term Single Spin Logic(SSL) was realized. The authors here propose a SSL made parallel 3-bit parity generator for Hamming code.

Index Terms—Single Spin Logic Parity generator,Hamming code, Anti-ferromagnetic, Robustness,Powerconsumption,Not interconnected

1 Introduction

Hamming code is the brainchild of Richard W Hamming and it was modelled in the Bell labs [1].The Hamming code is the use of extra parity bits to signify the error.The effectiveness of Hamming code is that i) It achives Highest possible rates for codes, ii)It is a single error correcting code & iii)It can detect upto two bit of errors.Since long it is hard pressed to obtain Hamming code hardware using low power consuming devices.Also if the size of Hamming code hardware shrinked within few nm then obviously it can be fabricated in any communication devices. There have been reports of improvising hamming code hardware since the ast decade [2]. Most of theses are CMOS made. On the other handcharge coupled devices are facing physical constraints and thus less then 60nm ICs are not feasible within the existing Lithographic techniques [3].Different new topologies are attracting Researchers worldwide. In 1994 Prof. S. Bandyopadhyay first conceptualized Spintronics- a new paradigm that is totally different from any charge coupled devices. The Spin based devices are free from all the limitations of conventional charge coupled devices as only the spin degree of freedom is considerd in Spin logic devices. Several research attempts are made so far to mimic the spin attributes in bolean logic [4], [5].

Here the authors intend to design next generation Hamming code circuit using Single Spin Logic(SSL).

2 The Proposed SSL Based Parity Bit Generator For Hamming Code

The 7 bit hamming code is modelled using SSL Six-XOR gates in fig.1 below.Each word of the code comprises of 7 single bits numberdthrough 1 to 7 for design clarity.Bits 1, 2, 4 are marked as parity bits (P_1,P_2,P_4 respectivly).Where as the messege bits are labled as (D_3,D_5,D_7respectivley).

The SSL parity bit generator for hamming code circuit is modelled in a fashion where each parity bits is in conjunction with 3 other message bits and forms a 4 bit word with even parity that is if P_1 is chosen as a 0 or 1 then P_1,D_3,D_5,D_7 will produce an even parity.Y_1 ,Y_2,Y_4 are add interim output.

The same is been reciprocated in table below:

TABLE-1		
$P_1=^0_1$	P_1 D_3 D_5 D_7	EVEN
$P_2=^0_1$	P_2 D_3 D_6 D_7	EVEN
$P_4=^0_1$	P_4 D_5 D_6 D_7	EVEN

We can obtain any parity bit with 3 message bits from the given table above.The parity bit will be 1 only if the no of 1's in the 3 message bit is an odd one i.e a single one or three ones.

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3 COMPARATIVE STUDY OF CONVENTIONAL HAMMING CODE & SSL HAMMING CODE:

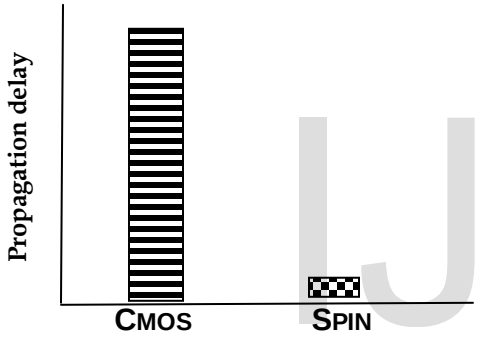
The authors relied upon the empirical results obtained during the analytical study of the proposed SSL made parallel 3-bit parity generator for Hamming code. The numerical results in the following categorically demonstrate the advantages of SSL over conventional CMOS.

COMPARISION FASTNESS OF VARIOUS SEMI CONDUCTOR DEVICE-

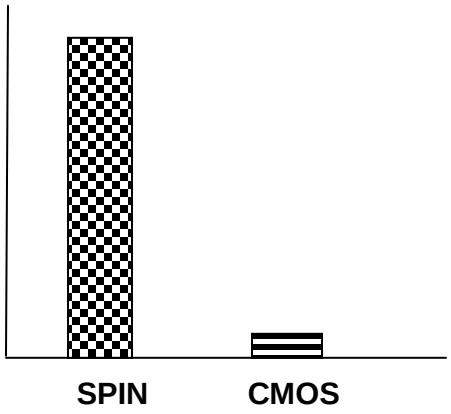
TABLE-2

	Device Name	Propagation delay time	FASTER (time)with respect to CMOS
1	CMOS	12ns	1
2	SSL	1ps	12000

GRAPHICAL REPRSENTATION



COMPARISION OF PROPAGATION DELAY



COMPARISION OF FASTNESS

COMPARISION OF POWER DISSIPATION PER GATE OF VARIOUS SEMI CONDUCTOR DEVICES

TABLE-3

SL NO	CIRCUIT NAME	POWER DIS-SIPATION	CONSUMING POWER W.R.T. CMOS
1	CMOS BASED	0.01/10-12 mW	1
2	SSL BASED	~50Nw	10^6

4 CONCLUSION

Due to size limitations conventional CMOS technology is fast approaching to its limits. Concequently novel technologies distinct from charge based technologies that has attracted researchers world-wide. Spin is a promising technology that doesn't involve charge base operation but produces negligible time delay and has no inter connection. Also the power consumption is drastically reduced and its memory is non-volatile one. Our designed SSL based parallel 3 bit parity generator Hamming code produces propagation delay of 1ps which is negligible and it is 12000 times faster than conventional CMOS based devices. SSL based device consumes less power (10^6) than the conventional CMOS based device.

The authors belive that the proposed SSL based parallel 3 bit Parity generator Hamming Code is a unique structure and can be easily included in the next generation Communication System.

Acknowledgment

Dr. JayantaGope on behalf of his students thankfully acknowledges the financial contribution provided by Director CSET.

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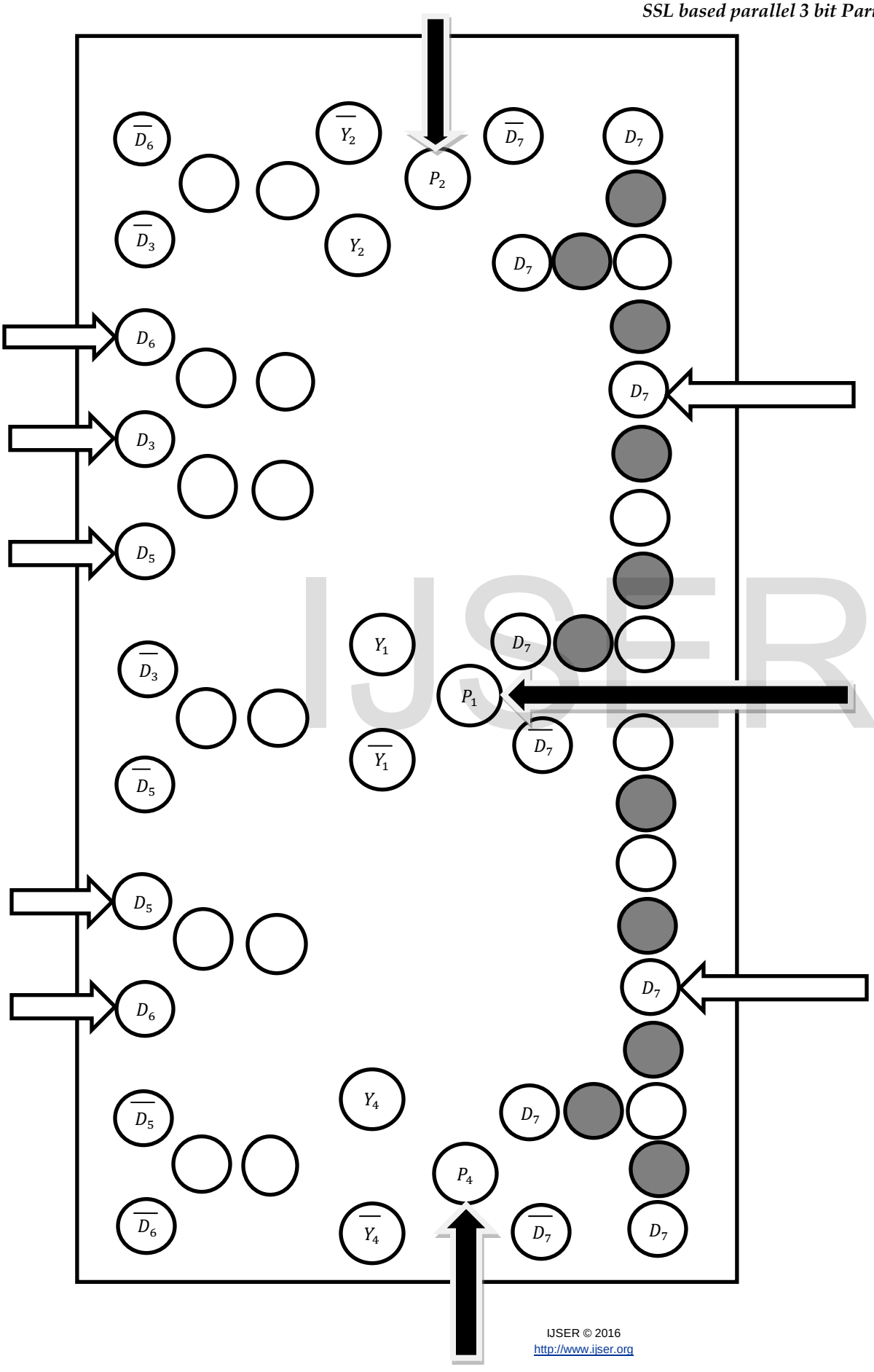
$\overline{D_6}$
$\overline{Y_2}$
P_2
$\overline{D_7}$
D_7
$\overline{D_3}$
Y_2
D_7
D_6
D_7
D_3
D_5
Y_1
D_7
$\overline{D_3}$
P_1
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Y_4
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P_4
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D_7